REMARKS

The Office Action of March 25, 2009 was received and carefully reviewed. Claims 1-14 were pending prior to the instant amendment. By this amendment, claims 1-4, 8-9, 11-12 and 14 are amended; claims 15-18 are added. Consequently, claims 1-18 are currently pending in the instant application. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yudasaka et al. (U.S. Patent Application Publication No. 2002/0179906, hereinafter "Yudasaka") in view of Bojkov et al. (U.S. Patent No. 5,947,783 hereinafter "Bojkov").[1] Yudasaka in view of Bojkov, however, fails to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claim **1** recites a combination that includes, among other things:

> *". . . a gate electrode formed over the one of the pair of substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and silicon nitride oxide formed on and in direct contact with the gate electrode . . . a gate insulating layer at least comprising a second layer including silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer."*

Independent claim **2** recites yet another combination that includes, *inter alia*,

> *". . . a gate electrode formed over the one of the pair of substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and silicon nitride oxide formed on and in direct contact with the gate electrode . . . a gate insulating layer at least comprising a second layer including silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer . . . wiring connected to at least one of a source and a drain . . . third layer including at least one of silicon nitride and silicon*

[1] Although the Examiner lists claims 1-13 being rejection (e.g., see page 2, item 2 of the present Office Action), it appears that claim 14 is also rejected over Yudasaka in view of Bojkov, as referenced in the final paragraph on page 5.

oxide formed on and in direct contact with the wiring . . . wherein the wiring is formed by fusing conductive nanoparticles."

Independent claim **3** recites a further combination that includes, for instance,

". . . the gate electrode formed over the one of the pair of substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and silicon nitride oxide formed on and in direct contact with the gate electrode . . . a gate insulating layer at least comprising a second layer including silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer."

Independent claim **4** recites another combination that includes, for instance,

" . . . a pixel electrode connected to the first thin film transistor . . . a first wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises:

". . . a driver circuit constructed by a second thin film transistor which comprises the same layer structure as the first thin film transistor . . . a first wiring extending from the driver circuit and connected to a gate electrode of the first thin film transistor, wherein the first thin film transistor comprises . . . the gate electrode formed over the one of the pair of substrates by fusing conductive nanoparticles . . . a first layer including at least one of silicon nitride and silicon nitride oxide formed on and in direct contact with the gate electrode . . . a gate insulating layer at least comprising a second layer including silicon oxide over the first layer . . . a semiconductor layer over the gate insulating layer . . . a second wiring connected to at least one of a source and a drain . . . a third layer including at least one of silicon nitride and silicon oxide formed on and in direct contact with the second wiring, wherein the second wiring is formed by fusing conductive nanoparticles."

Independent claim **11** recites another combination that includes, for example,

". . . forming a gate electrode over a substrate having an insulating surface with a droplet discharge method using a composition containing conductive nanoparticles . . . etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer by using the second mask . . ."

And finally, independent claim **12** recites a further combination that includes, for instance,

". . . forming a gate electrode and a connection wiring over a substrate having an insulating surface with a droplet discharge method using a composition containing conductive nanoparticles . . . etching the

semiconductor layer containing one conductivity type impurity and the semiconductor layer by using the second mask . . ."

At the very least, Yudasaka in view of Bojkov, whether taken alone or in combination, fail to disclose or suggest any of these exemplary features recited in independent claims 1-4 and 11-12.

For example, as for claims 1-4, on page 2 of the outstanding Office Action, the Examiner readily admits that Yudasaka fails to disclose a gate electrode formed by fusing conductive nanoparticles. The Examiner turns to the teachings of Bojkov in an attempt to cure the deficiencies of Yudasaka. The Examiner alleges that Bojkov discloses a gate electrode formed over a substrate by fusing conductive nanoparticles. As explained on page 6, paragraph 3 of the outstanding Office Action, the Examiner concludes that Bojkov teaches fusing conductive nanoparticles based upon Bojkov at col. 5, lines 41-50 which describes a continuous diamond layer 1801 formed by the process of diamond nucleation which occurs primarily onto the diamond particles. As argued in the previous response, Bojkov describes that the result of the process effectively reduces, or eliminates cross-talk between metal lines 1102. Thus, assuming *arguendo* that it would be possible to combine Bojkov with Yudasaka, it should be regarded that the diamond of Bojkov is not conductive and, in fact, teaches **away** (emphasis added) from the invention as claimed. Thus, Bojkov does not disclose or fairly suggest that the gate electrode is formed over the substrate by fusing conductive nanoparticles as recited, at least, in claims 1-4, and cannot cure the deficiencies of Yudasaka.

Moreover, Bojkov merely discloses a cathode assembly that can be used for a lamp, whereas the subject application claims a liquid crystal display device including a thin film transistor having a gate electrode formed by fusing conductive nanoparticles. Bojkov fails to disclose or fairly suggest a gate electrode formed by fusing conductive nanoparticles in a thin film transistor, as recited by the claims of the present invention. Additionally, on page 3,

line 8 of the present Office Action, the Examiner purports that Bojkov discloses a first layer including at least one of silicon nitride and silicon oxynitride . . . a gate insulating layer at least comprising a second layer including silicon oxide over the first layer. Applicant disagrees with this assertion. The subject application discloses a gate insulating layer having a layered structure (a first layer including at least one of silicon nitride and silicon nitride oxide and a gate insulating layer at least comprising a second layer including silicon oxide over the first layer). In contrast, however, Bojkov merely disclose only a dielectric or insulating material comprised of SiOx, SiNy, silicon oxi-nitride, or a metal oxide deposited onto the intersecting portions of a grid (e.g., see col. 3, lines 12-15). Furthermore, Bojkov is silent with regard to providing a description about a gate insulating layer or a gate insulating layer having a layered structure including the claimed materials.

Regarding claims 11 and 12, the cited prior art does not disclose or fairly suggest, alone, or in proper combination, at least, forming a gate electrode with a droplet discharge method using a composition containing conductive nanoparticles.

In accordance with the M.P.E.P. § 2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 409 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 196 (CCPA 1970). Therefore, it is respectfully submitted that neither Yudasaka nor Bojkov, taken alone or in any proper combination, discloses or suggests the subject matter as recited in claims 1-4 and 11-12. Hence, withdrawal of the rejection is respectfully requested.

Each of the dependent claims depend from one of independent claims 1-4 or 11-12 and are patentable over the cited prior art for at least the same reasons as set forth above with

respect to claims 1-4 and 11-12. In addition, each of the dependent claims also recites combinations that are separately patentable.

Newly added claims 15-18 depend from one of independent claims 11 or 12 and are patentable over the cited prior art for at least the same reasons as set forth above with respect to claims 11 and 12. (Support for the aforementioned claims is found, at least in lines 1-2 of paragraph [0037], lines 1-3 of paragraph [0057], lines 1-2 of paragraph [0052], lines 2-3 of paragraph [0071], and lines 1-3 of paragraph [0055] of the corresponding US Patent Application Publication.) In addition, each of the dependent claims also recites combinations that are separately patentable.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore requests the entry of this response, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

In discussing the specification, claims, and drawings in this response, it is to be understood that Applicant in no way intends to limit the scope of the claims to any exemplary embodiments described in the specification and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

NIXON PEABODY, LLP

/Marc W. Butler, Reg. #50,219/
Marc W. Butler
Registration No. 50,219

NIXON PEABODY LLP
CUSTOMER NO.: 22204
401 9th Street, N.W., Suite 900
Washington, DC 20004
Tel: 202-585-8000
Fax: 202-585-8080